Discussion

The Present Invention

- The structure to be corrected can be a chip; a package of chips; or an assembly of chips and/or packages on a board. Thus a "part" can be a chip; a package of chips; or an assembly of chips and/or packages on a board
- Each structure is designed to a "target" memory capacity without inclusion of spare data lines;
- Multiple defects in a structure can be corrected;
- A corrected memory end product comprises a "main" part, an independent "backup" part, and a correcting pattern of interconnection of the data lines with the data I/O connections of the end product.
- Correction is accomplished by substitution of an operational data line of a "backup" part for a defective line of a "main" part.

Daughton

- The only structure to be corrected is a monolithic chip;
- The I/O data lines of one chip cannot be used to replace a failed line of another chip.
- Only a single defect in a chip can be corrected;
- A corrected memory end product comprises a single chip mounted on a substrate in a package;
- Each structure includes a spare data line in addition to the planned "target" memory capacity;
- Correction is accomplished by redirection of cell address signals from a defective cell line to the "spare" cell line of the chip, along with circuitry for sensing signals from the spare line.
- Daughton, at column 9, lines 20 -43, suggests use of their claimed invention in the context of the prior art "three quarter good" arrangements wherein a quadrant of a chip is replaced. Such arrangements are not relevant to applicant's claimed invention.

The Claims as Amended

Each of the independent claims 1, 8, 12, and 50 are amended herein to clearly demonstrate that a working line or lines of one independent memory unit, i.e., a chip, a package, etc. are substituted for a failed line or lines of a different memory unit, again, i.e. a chip, a package, etc.

For example, claim 1 twice amended specifies:

> "— testing a plurality of independent memory parts for failed I/O data line segments;
>
> sorting the parts according to the results of the testing;
>
> identifying failed and working I/O data line segments in the sorted parts;
>
> selecting at least one primary part having at least one I/O data line failure, and at least one different partially defective backup memory part from said sorted parts; and
>
> combining working I/O data line segments of different selected memory parts, including at least one working I/O data line segment of at least one partially defective backup memory part and working I/O data line segments of a primary part—"

Independent claim 8, twice amended, specifies:

"A method for developing effective chip-on-board memory modules comprising an assembly of a selected combination of independent partially defective memory chips

comprising the steps of:

assembling the selected chips as primary chips and backup chips onto a chip-on-board memory module assembly;

testing the assembled module for failed I/O data lines in the chips;

identifying operating I/O data line segments in the chips; and

combining identified working I/O data line segments of a partially defective primary chip with a required number of working I/O data line segments of backup memory chips."

Independent claim 12, twice amended, similarly distinguishes over Daughton as follows:

A process for patching selected partially defective independent primary memory parts with selected different partially defective independent backup memory parts to form a memory module functionally transparent to the user, comprising the steps of:

testing the primary memory parts and the backup memory parts before mounting the parts on a board to;

identify operating and failed I/O data line segments of the primary parts and of the backup memory parts;

determining which operating I/O data lines from the backup memory parts to use for selectively patching failed I/O data lines segments of the primary memory parts; and

substituting said determined operating I/O data lines from the backup parts for failed I/O data l lines in one or more primary parts to form a completed memory module. "

Independent claim 50, twice amended, similarly distinguishes over Daughton.

selecting, as primary parts, partially defective dies that have a reasonable probability of being patched successfully;

selecting, as backup parts, other partially defective dies that test to be suitable for patching;

assembling the selected primary and backup parts on the PC module;

applying a plastic over coating to the assembled parts; and

testing the module using a chip test applied at the module pins; and

patching failed segments of the primary parts with working segments of the backup parts.

Independent claim 1 as originally presented specifies:

71. A method for constructing a fully functional memory module which utilizes partially defective independent memory circuit parts comprising:

(a) testing and classifying memory parts in a set of defined classifications

(b) selecting a primary memory part having a selected classification;

(c) selecting a backup memory part having a selected different classification; and

6 (d) constructing a memory module wherein: any defective data lines of the selected primary
7 memory part are replaced by operational data lines of the backup circuit structure.

Applicant respectfully submits that the amendments to the claims presented herein overcome: (a) the Examiner's objections to claims 33; (b) the basis of rejection of claims 1 - 18, 50, - 52, 68-73, and 75 under 35 U.S.C. 102(b) as anticipated by Daughton. Each of the independent rejected claims, namely 1, 8, 12, and 50, and 71, as now amended, distinguishes applicant's invention over Daughton and over any prior art known to the applicant.

Applicant respectfully requests entry of the amendments presented herein; reversal of the various objections and rejections presented in the present office action; and allowance of claims 1 - 64 and 67 - 75 as now presented.

Should the Examiner be of the view that a telephone or personal interview would be helpful in advancing prosecution of this application, the undersigned will welcome a call at (630) 377 2415. If I am not in my office, please leave a message on my answering machine.

Respectfully,

John C Albrecht December 21, 1999

John C. Albrecht (Reg. 18,373)